IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Kohler et al.
Case:	10-31-39
Serial No.:	11/586,176
Filing Date:	April 6, 2007
Group:	2827
Examiner:	Fernando N. Hidalgo
Title:	Method and Apparatus for Hot Carrier Programmed One Time Programmable (OTP) Memory

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants hereby appeal the final rejection, dated January 8, 2009 of claims 1-31 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded on April 6, 2007 in the United States Patent and Trademark Office at Reel 019127, Frame 0364. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on April 6, 2007 with claims 1 through 31. Claims 1 through 31 are presently pending in the above-identified patent application. Claims 1-5, 7-15 and

17-31 are rejected under 35 U.S.C. §103(a) as being unpatentable over Reiner (WO 2004/053889) in view of Lee (United States Patent No. 5,257,225) and Doyle et al. (U.S. Publication: "Characterization of Oxide Trap and Interface Trap Creation During Hot-Carrier Stressing of n-MOS Transistors Using the Floating-Gate Technique"; hereinafter Doyle).

The Examiner has indicated that claims 6 and 16 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Claims 1-5, 7-15 and 17-31 are being appealed.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 requires a method for programming a one time programmable memory (FIG. 5A, 500; FIG. 6A, 600; page 4, lines 20-23 and lines 28-31; page 5, lines13-20; page 6, lines 6-12), comprising the steps of: obtaining an array of transistors (FIG. 2, 200; page 3, lines 26, to page 4, line 3); and programming at least one of said transistors (FIG. 2, 200; FIG. 3, 310; FIG. 4, 400; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 7-9) using a hot carrier transistor aging technique (FIG. 2, 200; page 4, lines 7-9; page 5, lines 15-18; page 6, lines 8-10) to alter a characteristic of said at least one of said transistor (page 4, lines 7-9, lines 14-16, and lines 28-31; page 5, lines 15-20; page 6, lines 8-12), wherein the hot carrier aging technique comprises injection of carriers into a gate oxide (page 4, lines 11-12), and wherein the injection of carriers causes at least one of, the creation of traps (page 4, lines 13-14; page 5, lines 18-20; page 6, lines 10-12), and the filling of traps (page 4, lines 13-14).

Independent claim 11 requires a one time programmable memory (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 3, lines 24-25; page 5, lines 13-14; page 6, lines 6-7), comprising an array of transistors (FIG. 2, 200; page 3, lines 26, to page 4, line 3), wherein at least one of said transistors is programmed (FIG. 2, 200; FIG. 3, 310; FIG. 4, 400; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 7-9) using hot carrier transistor aging (FIG. 2, 200; page 4, lines 7-9; page 5, lines 15-18; page 6, lines 8-10) to alter a characteristic of said at least one of said transistor (page 4, lines 7-9, lines 14-16, and lines 28-31; page 5, lines 15-20; page 6, lines 8-12), wherein the hot carrier aging comprises

injection of carriers into a gate oxide (page 4, lines 11-12), and wherein the injection of carriers causes at least one of, the creation of traps (page 4, lines 13-14; page 5, lines 18-20; page 6, lines 10-12), and the filling of traps (page 4, lines 13-14); and a circuit for sensing said altered characteristic of said at least one of said transistor (FIG. 5B, 500; FIG. 6B, 600; page 4, lines 31-33; page 5, line 21, to page 6, line 5; page 6, lines 13-22).

Independent claim 21 requires a one time programmable memory element (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 3, lines 24-25; page 5, lines 13-14; page 6, lines 6-7), comprising at least one transistor that is programmed (FIG. 2, 200; FIG. 3, 310; FIG. 4, 400; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 7-9) using hot carrier transistor aging (FIG. 2, 200; page 4, lines 7-9; page 5, lines 15-18; page 6, lines 8-10) to alter a transistor characteristic (page 4, lines 7-9, lines 14-16, and lines 28-31; page 5, lines 15-20; page 6, lines 8-12), wherein the hot carrier aging comprises injection of carriers into a gate oxide (page 4, lines 11-12), and wherein the injection of carriers causes at least one of, the creation of traps (page 4, lines 13-14; page 5, lines 18-20; page 6, lines 10-12), and the filling of traps (page 4, lines 13-14); and a circuit for sensing said altered characteristic of said transistor (FIG. 5B, 500; FIG. 6B, 600; page 4, lines 31-33; page 5, line 21, to page 6, line 5; page 6, lines 13-22).

Independent claim 24 requires a memory cell, comprising only one transistor (FIG. 4, 400; FIG. 5A, 500; FIG. 5B, 500; FIG. 6A, 600; FIG. 6B, 600; page 5, lines 13-14; page 6, lines 6-7), wherein said transistor comprises: a source region (FIG. 4, 430; page 5, lines 1-6); a drain region (FIG. 4, 440; page 5, lines 1-6); a channel region (FIG. 4, 480; page 5, lines 1-6); one silicon-dioxide gate insulator layer (FIG. 4, 460; page 5, lines 1-6); and one gate electrode layer (FIG. 4, 470; page 5, lines 1-6).

Independent claim 27 requires an integrated circuit (page 3, lines 26-27), comprising: a one time programmable memory (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 3, lines 24-25; page 5, lines 13-14; page 6, lines 6-7), comprising an array of transistors (FIG. 2, 200; page 3, lines 26, to page 4, line 3), wherein at least one of said transistors is programmed (FIG. 2, 200; FIG. 3, 310; FIG. 4, 400; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 7-9) using hot carrier transistor aging (FIG. 2, 200; page 4, lines 7-9; page 5, lines 15-18; page 6, lines 8-10) to alter a characteristic of said at least one of said transistor (page 4, lines 7-9, lines 14-16, and lines 28-31; page 5, lines 15-20; page 6, lines 8-12), wherein the hot carrier aging comprises injection of carriers into a gate oxide (page 4, lines 11-

12), and wherein the injection of carriers causes at least one of, the creation of traps (page 4, lines 13-14; page 5, lines 18-20; page 6, lines 10-12), and the filling of traps (page 4, lines 13-14); and a circuit for sensing said altered characteristic of said at least one of said transistor (FIG. 5B, 500; FIG. 6B, 600; page 4, lines 31-33; page 5, line 21, to page 6, line 5; page 6, lines 13-22).

Dependent claim 2 requires that said programming step further comprises the step of applying a stressful voltage to said at least one of said transistors (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 16-18, lines 20-23; page 5, lines 15-18; page 6, lines 8-10) to cause said hot carrier transistor aging (page 4, lines 16-18, lines 20-23; page 5, lines 15-18; page 6, lines 8-10).

Dependent claim 3 requires that wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors (page 4, lines 7-16, and lines 28-31; page 5, lines 15-20).

Dependent claim 4 requires that said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors (FIG. 5A, 500; page 4, lines 20-23; page 5, lines 16-18) to cause said change in said threshold voltage of said of said at least one of said transistors (page 4, lines 28-31; page 5, lines 16-18).

Dependent claim 5 requires that the step of detecting said programmed at least one of said transistors (FIG. 5B, 500; page 5, line 21, to page 6, line 5) by sensing said change in said threshold voltage of said at least one of said transistors (FIG. 5B, 500; page 5, line 21, to page 6, line 5).

Dependent claim 7 requires that said altered characteristic is a change in a saturation current of said at least one of said transistors (page 4, lines 7-16, and lines 28-31; page 6, lines 8-12).

Dependent claim 8 requires that said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistors (FIG. 6A, 600; page 4, lines 20-23; page 6, lines 8-10) to cause said change in said saturation current of said of said at least one of said transistors (page 4, lines 28-31; page 6, lines 8-10).

Dependent claim 9 requires that the step of detecting said programmed at least one of said transistors (FIG. 6B, 600; page 5, lines 21-28; page 6, lines 13-23) by sensing said change in said saturation current of said at least one of said transistors (FIG. 6B, 600; page 5, lines 21-28; page 6, lines 13-23).

Dependent claim 10 requires that said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive potential (FIG. 6B, 600; page

6, lines 13-18); raising a gate terminal of each transistor in a selected row to a positive potential (FIG. 6B, 600; page 6, lines 16-18) and evaluating a rate of voltage decay of at least one column in said array of transistors (FIG. 6B, 600; page 6, lines 18-22).

Dependent claim 12 requires that wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 16-18, and lines 20-23; page 5, lines 15-18; page 6, lines 8-10) to cause said hot carrier transistor aging (page 4, lines 16-18, and lines 20-23; page 5, lines 15-18; page 6, lines 8-10).

Dependent claim 13 requires that said altered characteristic is a change in a threshold voltage of said at least one of said transistors (page 4, lines 7-16, lines 28-31; page 5, lines 15-20).

Dependent claim 14 requires that said at least one of said transistors is programmed by applying a stressful voltage to a drain and a gate of said at least one of said transistors (FIG. 5A, 500; page 4, lines 20-23; page 5, lines 16-18) to cause said change in said threshold voltage of said of said at least one of said transistors (page 4, lines 28-31; page 5, lines 16-18).

Dependent claim 15 requires that said circuit senses said change in said threshold voltage of said at least one of said transistors (FIG. 5B, 500; page 5, line 21, to page 6, line 5).

Dependent claim 17 requires that said altered characteristic is a change in a saturation current of said at least one of said transistors (page 4, lines 7-16, and lines 28-31; page 6, lines 8-12).

Dependent claim 18 requires that said at least one of said transistors is programmed by applying a stressful voltage to a source and a gate of said at least one of said transistors (FIG. 6A, 600; page 4, lines 20-23; page 6, lines 8-10) to cause said change in said saturation current of said of said at least one of said transistors (page 4, lines 28-3; page 6, lines 8-10).

Dependent claim 19 requires that said circuit senses said change in said saturation current of said at least one of said transistors (FIG. 6B, 600; page 5, lines 21-28; page 6, lines 13-23).

Dependent claim 20 requires that said circuit raises a voltage on at least one column in said array of transistors to a positive potential (FIG. 6B, 600; page 6, lines 13-18); raises a gate terminal of each transistor in a selected row to a positive potential (FIG.2, 200; FIG. 6B, 600; page 6, lines 16-18) and evaluates a rate of voltage decay of at least one column in said array of transistors (FIG. 6B, 600; page 6, lines 18-22).

Dependent claim 22 requires that said altered characteristic is a change in a saturation current of said transistor (page 4, lines 7-16, lines 28-31; page 6, lines 8-12).

Dependent claim 23 requires that said altered characteristic is a change in a threshold voltage of said transistor (page 4, lines 7-16, and lines 28-31; page 5, lines 15-20).

Dependent claim 25 requires that the memory element is a one time programmable memory element (FIG. 5A, 500; FIG. 6A, 600; page 4, lines 20-23 and 28-31; page 5, lines13-20; page 6, lines 6-12) programmed (FIG. 2, 200; FIG. 3, 310; FIG. 4, 400; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 7-9) using a hot carrier transistor aging technique (FIG. 2, 200; page 4, lines 7-9; page 5, lines 15-18; page 6, lines 8-10) to alter a characteristic of said transistor (page 4, lines 7-9, lines 14-16, and lines 28-31; page 5, lines 15-20; page 6, lines 8-12), wherein the hot carrier aging technique comprises injection of carriers into a gate oxide (page 4, lines 11-12), and wherein the injection of carriers causes at least one of, the creation of traps (page 4, lines 13-14; page 5, lines 18-20; page 6, lines 10-12), and the filling of traps (page 4, lines 13-14).

Dependent claim 26 requires that a plurality of said memory cells arranged in an array of rows and columns (FIG.2, 200; page 3, line 26, to page 4, line 9).

Dependent claim 28 requires that said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors (FIG. 2, 200; FIG. 5A, 500; FIG. 6A, 600; page 4, lines 16-18, lines 20-23; page 5, lines 15-18; page 6, lines 8-10) to cause said hot carrier transistor aging (page 4, lines 16-18, lines 20-23; page 5, lines 15-18; page 6, lines 8-10).

Dependent claim 29 requires that said altered characteristic is a change in a threshold voltage of said at least one of said transistors (page 4, lines 7-16, and lines 28-31; page 5, lines 15-20).

Dependent claim 30 requires that said circuit senses said change in said threshold voltage of said at least one of said transistors (FIG. 5B, 500; page 5, line 21, to page 6, line 5).

Dependent claim 31 requires that said altered characteristic is a change in a saturation current of said at least one of said transistors (page 4, lines 7-16, and lines 28-31; page 6, lines 8-12).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appealed claims 1-5, 7-15 and 17-31 are rejected under 35 U.S.C. §103(a) as being unpatentable over Reiner in view of Lee and Doyle.

ARGUMENT

Independent Claims

Claims 1, 11, 21, 24 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Reiner in view of Lee and Doyle.

Regarding claims 1 and 2, the Examiner states in the final Office Action dated January, 8 2009, that Reiner teaches programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistors (the Examiner asserts that Reiner at page 5, line 19, to page 6, line 19 discloses thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction), wherein the hot carrier aging technique comprises injection of carriers into a gate oxide (the Examiner asserts that Reiner at page 7, lines 7-11 discloses gate oxide breakdown as induced by hot carriers resulting from T2 being voltage/current biased as disclosed on pages 5-6).

The Examiner acknowledges that Reiner does not disclose that the injection of carriers causes at least one of the creation of traps and the filling of traps. The Examiner further states, in the Office Action, that Reiner teaches (at page 7, lines 7-11) oxide breakdown as obviously induced by degradation by hot carrier mechanism: trapping electrons.

The Examiner further states, in the Office Action, that Lee teaches in the context of OTP memory devices "filling up the traps in the dielectric region" (Lee at column 4, line 67, to column 5, line 2) and that Doyle teaches trap creation during hot carrier stressing of n-MOS transistors (Abstract of Doyle)

Appellants respectfully disagree with these statements.

Regarding the limitation of programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistors, Reiner does not disclose *programming* using *hot carriers*, but, rather, discloses *programming by thermally damaging the drain junction*. Reiner states that "a MOS transistor is employed as memory; this memory transistor can be *programmed* by being brought itself into a snap-back mode, in which a drain junction of the transistor is thermally damaged." (Reiner: page 2, lines 13-16). Reiner further states that "The device further comprises programming means for applying predetermined voltages ..., which applied voltages force the memory transistor into a snap-back mode resulting in a current thermally damaging the drain junction of the memory transistor." (Reiner at page 2, lines 4-8), "The

programming of the memory transistor results in a leakage in the transistor, which can be detected in the form of a leakage current in a subsequent readout. It should be ensured in the readout that a detected leakage is indeed caused by a *hard drain fusing which results in a damaged connecting the drain with the source diffusion*" (Reiner: page 4, lines 14-18), and "*Hot carrier conditions resulting in a degradation, however, are avoided effectively with the proposed programming cycle* comprising a ramping down of the voltage applied to the gate of the memory transistor." (Reiner: page 4, lines 7-9). Appellants specifically disagree with the assertion in the Office Action by the Examiner that Reiner (at page 5, line 19, to page 6, line 19) discloses thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction. Appellants note that the cited portion of Reiner does not disclose, teach, mention or indicate hot carriers. *Therefore, Reiner does not teach hot carrier aging techniques for programming a memory cell.*

Regarding the limitation that the hot carrier aging technique comprises injection of carriers into a gate oxide, Reiner does not disclose programming by injecting carriers into a gate oxide. Appellants specifically disagree with the assertion in the Office Action by the Examiner that Reiner, at page 7, lines 7-11, discloses gate oxide breakdown as induced by hot carriers resulting from T2 being voltage/current biased as disclosed on pages 5-6. The cited portion or Reiner recites:

> Experiments have shown that drain fusing occurs without an additional gate oxide breakdown with a certainty level of 90%. But even in case the gate oxide of a programmed memory transistor has broken down, this cell will still allow a leakage current and be considered as programmed. Therefore, the proposed memory is insensitive to gate oxide breakdown in a programmed cell.

The cited portion of Reiner mentions gate oxide breakdown, but does not disclose that hot carriers are a result of T2 being voltage/current biased as disclosed on pages 5-6. Furthermore, the cited portion of Reiner make clear that oxide breakdown, and consequently any inferred hot carriers, is not necessary or even desired for the programming of Reiner, to the contrary drain fusing is the programming mechanism of Reiner. Reiner recites that "the proposed memory is insensitive to gate oxide breakdown in a programmed cell." Reiner is clear that drain damage, not gate oxide breakdown (and any related inferred hot carriers), is the programming mechanism for the memory cell. Reiner never mentions hot carrier programming or the injection of any carriers into a gate oxide. *Therefore, Reiner does not disclose or suggest that a hot carrier aging technique comprises injection of carriers into a gate oxide to program a memory cell.*

Regarding the assertion in the Office Action by the Examiner that Reiner teaches, at page 7, lines 7-11, oxide breakdown as obviously induced by degradation by hot carrier mechanism: trapping electrons. Appellants disagree. Reiner never mentions or teaches oxide breakdown related to hot carriers, hot carrier mechanisms, degradation by hot carrier mechanisms, trapping electrons or traps.

Appellants further note that Reiner teaches:

> In an equally preferred embodiment of the invention, a programming voltage level above the normal operation voltage level is used, in order to keep the cell size reasonably small. *High voltage levels may result in a degradation of the memory device due to an increased heating of the carrier. Hot carrier effects occur e. g. in strong pinch-off conditions in a transistor, which in turn occur with a high drain voltage and a moderate to low gate voltage at the transistor. It has thus to be ensured that no intolerable degradation of the memory circuitry occurs due to the proposed high programming voltage. Hot carrier conditions resulting in a degradation, however, are* ***avoided effectively*** *with the proposed programming cycle comprising a ramping down of the voltage applied to the gate of the memory transistor.*
> (Page 3, line 31, to page 4, line 9; emphasis added.)

Thus, contrary to the Examiner's assertion, *Reiner does not disclose or suggest programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.* In fact, Reiner actually **teaches away** from the present invention by teaching to *avoid hot carrier conditions.*

In the Advisory Action dated March 23, 2009, on page 2, the Examiner, in regards to independent claims 1, 11, 21, and 27 and dependent claim 25, referencing Reiner at page 4, recites "That is, unquestionably and objectively clear that hot carrier effects occur and that intolerable degradation (memory rendered useless in plain language) occurrence is to be avoided. … Reiner, in fact, teaches programming, wherein hot carrier effects occur, but sensibly caution that no INTOLERABLE DERADATION be permitted." Appellants assert that, while Reiner may arguably mention the possibility of hot carrier effects occurring, the memory of Reiner does not *use those hot carrier effects to program the memory.* Reiner states on page 4, lines 7-9, that "Hot carrier conditions resulting in a degradation, however, are avoided effectively with the proposed programming cycle." Appellants note that it is precisely that or similar degradation (e.g., change in threshold voltage, change in saturation current, creation of traps and filling of traps) that is claimed by Appellant for programming the memory using a hot carrier aging technique.

Lee and Doyle

Furthermore, in the text cited by the Examiner (Lee at col. 4, line 67, to col. 5, line 2), Lee teaches "the fact that wordline pulse 65 ramps up is significant is that the small Fowler-Nerdheim current at the beginning which fills up the traps in the thin dielectric region before the higher Fowler-Nerdheim current will reduce the stress on the tunneling window dielectric and improve the dielectric lifetime." (Col. 4, line 67, to col. 5, line 4.) Lee, however, does not disclose or suggest programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.

Finally, Doyle does not disclose or suggest programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.

Thus, even as combined in the manner suggested by the Examiner, Reiner, Lee and Doyle, alone or in combination, *do not teach every element of the independent claims*. Furthermore, based on the KSR considerations discussed hereinafter, the combination/modification suggested by the Examiner is not appropriate.

KSR Considerations

An Examiner must establish "an apparent reason to combine … known elements." *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. ___, 82 USPQ2d 1385 (2007). Here, the Examiner merely states that it would have been obvious to incorporate the teachings (that the injection of carriers causes at least one of, the creation of traps, and the filling of traps) by Lee and Doyle in the cited claim limitation rejection. In the Office Action, the Examiner asserts that the suggestion/motivation would have been obvious to one of ordinary skill in the art to conclude that (the) injection of carriers, as induced by voltage/current biasing of a transistor device, can cause oxide degradation resulting in charge trapping.

Appellants, however, are claiming a new technique for programming a one time programmable memory. There is no suggestion in Reiner, Lee and Doyle, alone or in combination, to *program a transistor using a hot carrier transistor aging technique to alter a characteristic of the transistor.*

Furthermore, Reiner's teaching to *avoid hot carrier conditions* ***teaches away*** from the present invention. The *KSR* Court discussed in some detail United States v. Adams, 383 U.S. 39 (1966), stating in part that in that case, "[t]he Court relied upon the corollary principle that when the prior art

teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." (KSR Opinion at p. 12). Thus, there is no reason to make the asserted combination/modification.

Regarding claims 11, 21, and 27, which include limitations similar to claim 1, Appellants apply the same arguments as asserted for claim 1.

Regarding claim 24, which recites a "memory cell, *comprising only one transistor*," the Examiner in rejecting claim 24 recites that Reiner teaches a memory cell comprising only one transistor (Reiner at page 5, line 9; T2 of FIG. 1). Appellants disagree and note that Reiner states "The memory cell comprises a selection transistor T1 and a memory transistor T2" (Reiner: page 5, lines 8 and 9). Furthermore, Reiner states "FIG. 1 schematically illustrates a memory cell of a memory device according to the invention" (Reiner: page 5, lines 3 and 4). FIG. 1 clearly shows two transistors, T1 and T2, within the illustrated memory cell. Thus, the memory cell of Reiner does not comprise only one transistor, but comprises two transistors.

In the Advisory Action on page 2, regarding claim 24, the Examiner further recites that Reiner, at least on page 5, teaches "a memory transistor T2," that a select transistor for selectively programming the one memory transistor is available, and that this is no different from the instant application, wherein in at least the abstract and paragraph [0006] it is disclosed that "transistors on the array are selectively programmed." Application assert that, in regard to the number of transistors comprised in the memory cells, a distinction between the memory cell of Reiner and an exemplary memory cell of Appellant is at least that Appellant does not have a select transistor separate from the transistor that stores the state of the memory (storage transistor or memory transistor), and Reiner has separate select and storage (memory) transistors. The single-transistor memory cell of Appellants is illustrated as 210-1,1; 210-1,2; 210-2,1 and 210-2,2 in the array of memory cells 200 of FIG. 2 (see specification of Appellant at page 3, line 26, to page 4, line 3). Reiner illustrates a memory cell in FIG. 1 (see Reiner at page 5, lines 1-2; and lines 7-15). Reiner recites at page 5, lines 7-8 "Figure 1 shows an OTP memory cell forming part of a CMOS memory according to the invention. The memory cell comprises a selection transistor T1 and a memory transistor T2." Clearly the memory cell of Rainer comprises two transistors, and an exemplary memory cell of Appellants is a single-transistor memory cell. Furthermore, Appellants disagree with the assertion by the Examiner that "there is absolutely no way, technique, manner or method that would program a one transistor

memory without means for first selecting it for applying voltage biasing conditions." For an exemplary memory cell of Appellants included within an array (e.g., array 200 of FIG. 2), the application of a stress voltage on one row (e.g., ROW 1) and the simultaneous application of another stress voltage on one column (e.g., COLUMN 2) uniquely selects a one-transistor memory cell (e.g., cell 210-1,2) for programming. Therefore, Reiner, Lee and Doyle, alone or in combination, do not disclose a memory cell comprising only one transistor.

With further regard to claim 27 which requires an integrated circuit, in the Office Action, the Examiner in rejecting claim 27 does not present any teachings or disclosure of an integrated circuit. At least because the Examiner does not present a teaching or disclosure of an integrated circuit, the Appellants believe that claim 27 is in condition for allowance.

In the Advisory Action on page 2, regarding claim 27, the Examiner asserts that the OTP memory and associated means of Reiner are inherently parts of an integrated circuit. Appellants still assert that Reiner does not teach an integrated circuit. Furthermore, other alternatives are available, for example, the OTP memory and associated means may comprise discrete semiconductor devices and other discrete electronic devices such as discrete transistors, resistors, capacitors, and interconnects. Therefore, Reiner does not teach an integrated circuit.

Thus, Reiner, Lee and Doyle, alone or in combination, do not disclose or suggest a method, a one time programmable memory, a memory cell, an integrated circuit, or other apparatus for programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps, as required by each of independent claim 1, 11, 21 and 27 and by dependent claim 25 dependent upon independent claim 24.

Dependent Claims

Claims 2-10, 12-20, 22-23, 25-26 and 28-31 are dependent on one of independent claims 1, 11, 21, 24 and 27, and are therefore patentably distinguished over Reiner, Lee and Doyle, alone or in combination, because of their dependency from independent claims 1, 11, 21, 24 and 27 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

Dependent Claims 2-5, 7-10, 12-15, 17-20, 22-23, 25-26 and 28-31 are being appealed.

With regard to claims 2, 12 and 28, in the Office Action, the Examiner does not assert specific teachings of Reiner, Lee or Doyle that teach applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging. Appellants assert that Reiner, Lee and Doyle, alone or in combination, do not teach that said programming step further comprises the step of applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

In rejecting claims 3, 13, 23 and 29, the Examiner recites in the Office Action that "Reiner teaches said altered characteristics is a change in a threshold voltage of said at least one of said transistors (page 6, lines 27-31 teach that T2 of FIG. 1, when not programmed in a reading operation, will not conduct current; yet when T2 is programmed, in contrast, it will conduct current, obviously changing the threshold voltage of the memory T2)." Appellants disagree and note that Reiner states "a current should flow through the cell even though the memory transistor T2 is turned off, since the fused drain junction of the memory transistor T2 allows a leakage current to pass" (Reiner: page 6, lines 29-31). Appellants assert that if the memory transistor T2 is turned off (i.e., the gate voltage is below for NMOS transistors, or above for PMOS transistors, the threshold voltage of the transistor), conduction in the transistor T2 is not related to threshold voltage or a change in threshold voltage. Appellants further note that Reiner states "while in a programmed state of the memory cell, the drain junction of the memory transistor T2 is thermally damaged." (Reiner: page 5, lines 17-18). Therefore, the current conducted is not due to a change in threshold voltage, but to drain leakage current caused by the fused drain. As is known in the art, threshold voltage is the gate voltage at which channel conduction occurs between the source and drain of the transistor. Threshold voltage is not a voltage at which drain leakage occurs. Therefore Reiner does not teach said altered characteristic is a change in a threshold voltage.

In the Advisory Action on page 2, regarding claims 3, 13, 23 and 29, which require that said altered characteristic is a change in a threshold voltage of said at least one of said transistors, the Examiner asserts that Reiner teaches on page 7 "that programming of the memory cell can be determined by the amount of current passing through the memory channel: below a predetermined detection level is considered no programming, above said level is considered programming." In fact, what Reiner teaches on page 7 is "A cell with a detected current lying below a predetermined detection level is considered not to be programmed, wherein a cell with a detected current lying above a predetermined detection level is considered to b programmed." Reiner makes no mention of current

passing through a memory channel. Because Reiner does not teach current passing through a memory channel, and because threshold voltage is the gate voltage at which channel conduction occurs between the source and drain of the transistor, Reiner does not teach that said altered characteristic is a change in a threshold voltage of said at least one of said transistors. Although, as the Examiner asserts, that threshold voltage can be in direct relationship to the current through a transistor channel, there may be other parameters that are also in direct relationship to the current through a transistor channel, e.g., drain to source voltage. Besides, the programming of Reiner does not modulating channel current; therefore, modulation of drain current by the programming of Reiner is not associated with channel current or threshold voltage.

In rejecting claims 4 and 14, in the Office Action, the Examiner recites that Reiner teaches said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors (page 5, line 7, to page 7, line 6). Appellants disagree and note that, if any stressful voltage is applied, the stressful voltage is applied only to a drain, not to a gate. Reiner states "The programming voltage Vprog is set to a level exceeding the allowed maximum operating voltage" (Reiner: page 5, lines 24-25). FIG. 1 of Reiner shows Vprog applied to the drain of T1. Reiner further states "For programming a memory cell, the voltages Vsel and Vctrl applied to the gate of the selection transistor T1 and to the gate of the memory transistor T2, respectively, are set by programming means (not shown) to a voltage level predetermined for programming." (Reiner: page 5, lines 19-22). Appellants note that Reiner does not mention a stressful voltage applied to a gate. Furthermore, as noted with respect to claim 3, Reiner does not teach a change in threshold voltage. Thus, Reiner does not teach programming comprising applying a stressful voltage to a drain and a gate of a transistor to cause a change in threshold voltage of the transistors.

In the Advisory Action on page 2, in regards to claims 4 and 14, the Examiner referring to page 4 of Reiner and the recitation by Reiner of a moderate gate voltage, asserts that Reiner discloses programming using stressful voltages applied the gate. Appellants note that Reiner, at page 4, lines 2-9, recites that high voltage levels may result in degradation, and that hot carrier effects occur with a high drain voltage and a moderate to low gate voltage. *High voltage levels that may result in degradation* indicate that high voltage levels are stressful and that moderate to low voltage levels are not stressful. Reiner then proceeds to recite that hot carrier degradation are avoided by the proposed programming

cycle of Reiner. Thus, Reiner is not specifying that the programming methods of Reiner use the moderate to low gate voltage. Reiner, at page 5, lines 24-26 specifically specifies the stressful programming voltage: "the programming voltage Vprog is set to a level exceeding, the allowed maximum operating voltage of the employed CMOS technology." FIG. 1 of Reiner shows Vprog applied to the bitline (BL), thus, at least partially applied to the drain of T2. The gate voltage (Vctrl of FIG. 2) is not taught by Reiner as exceeding the maximum operating voltage or otherwise being at a sufficiently high voltage level to be stressful.

In rejecting claims 5, 15 and 30, the Examiner recites in the Office Action that Reiner teaches the step of detecting said programmed at least one of said transistor by sensing said change in said threshold voltage of said at least one of said transistors (page 6, line 27, to page 7, line 6). Per Appellants argument set forth regarding claims 3 and 4 above, Reiner does not teach a change in threshold voltage. Furthermore, Reiner does not teach a detection of a change in threshold voltage. On page 6, lines 27-31, Reiner teaches the change in current is due to leakage of the fused drain junction of T2, not a change in threshold. Reiner states "since the fused drain junction of the memory transistor T2 allows a leakage current to pass. The amount of current flow is detected" (Reiner: page 6, lines 30, to page 7, line 1). Thus, Reiner does not teach detecting said programmed at least one of said transistors by sensing said change in said threshold voltage of said at least one of said transistors.

In the Advisory Action on page 2, in regards to claims 5 and 15 and 30, the Examiner referring to page 6 of Reiner, asserts that Reiner teaches a subsequent readout of the memory by readout means (sensing detection) of the current (thus threshold) of the memory. In fact, at page 6, lines 20-21, Reiner recites: "A subsequent readout of the memory transistor T2 is performed by readout means (not shown) sensing a leakage current in the memory cell." Reiner does not teach "threshold" or readout of the memory by sensing detection of a threshold of the memory. Reiner goes on to recite, at page 6, lines 22-26, that "To this end, the readout means apply ...., while the memory transistor T2 is not turned on." Appellants assert that if the memory transistor T2 is not turned on, then the gate voltage applied to T2 is below the characteristic threshold voltage of transistor T2, and therefore, the threshold voltage of T2 is not material to the readout of the data state of T2 (i.e., the readout of the data state is not dependent upon the threshold voltage).

In rejecting claims 7, 17, 22 and 31, the Examiner recites in the Office Action that Reiner teaches that said altered characteristic is a change in a saturation current of said at least one of said

transistors (page 6, lines 26, to page 7, line 6). Reiner does not mention or teach saturation current. Reiner teaches the altered characteristic is a change in drain leakage current. Reiner states "a current should flow through the cell even though the memory transistor T2 is turned off, since the fused drain junction of the memory transistor T2 allows a leakage current to pass" (Reiner: page 6, lines 29-31). Appellants further note that Reiner states "while in a programmed state of the memory cell, the drain junction of the memory transistor T2 is thermally damaged." (Reiner: page 5, lines 17-18). As is well known in the art of transistors, saturation current is the channel current (i.e., the current flowing between source and drain) that flows when the gate to source voltage is greater than the threshold voltage, i.e., $V_{GS} > V_{th}$, and the drain to source voltage is greater than the gate to source voltage minus the threshold voltage, i.e., $V_{DS} > (V_{GS} - V_{th})$. Thus, Reiner does not teach said altered characteristic is a change in a saturation current of said at least one of said transistors.

In rejecting claims 8 and 18, the Examiner recites that Reiner teaches said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistor to cause said change in said saturation current of said of said at least one of said transistors (page 5-6). Appellants disagree and note that, if any stressful voltage is applied, the stressful voltage is applied to a drain, not to a gate (see above regarding claims 4 and 14). Reiner states "The programming voltage Vprog is set to a level exceeding the allowed maximum operating voltage" (Reiner: page 5, lines 24-25). FIG. 1 shows Vprog applied to the drain of T1. Reiner further states "For programming a memory cell, the voltages Vsel and Vctrl applied to the gate of the selection transistor T1 and to the gate of the memory transistor T2, respectively, are set by programming means (not shown) to a voltage level predetermined for programming." (Reiner: page 5, lines 19-22). Appellants note that Reiner does not mention a stressful voltage applied to a gate. Furthermore, as noted with respect to claim 7, Reiner does not teach a change in saturation current. Thus, Reiner does not teach said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

In rejecting claims 9 and 19, the Examiner recites in the Office Action that Reiner teaches the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors (page 6-7). Per Appellants argument set forth regarding claims 7 and 8 above, Reiner does not teach a change in saturation current. Furthermore,

Reiner does not teach a detection of a change in saturation current. In page 6, line 27 to line 31, Reiner teaches the change in current is due to leakage of the fused drain junction of T2, not a change in saturation current. Reiner states "since the fused drain junction of the memory transistor T2 allows a leakage current to pass. The amount of current flow is detected" (Reiner: page 6, lines 30, to page 7, line 1). Thus, Reiner does not teach detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors.

In rejecting claims 10 and 20, in the Office Action, the Examiner recites that Reiner teaches said detecting step further comprises the steps of raising the gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay if at least one column in said array of transistors (page 6, lines 22-23). Reiner does not teach or mention rows or raising the gate terminal of each transistor in a selected row. Thus, Reiner does not teach raising a gate terminal of each transistor in a selected row to a positive potential.

In the Advisory Action on page 2, in regards to claims 10 and 20, the Examiner asserts that memory elements of cells are inherently organized in rows and columns and that the teachings of Reiner on page 2 teach applying a gate voltage on a memory cell. Appellants assert that, as well known in the art, memory cells can be configured other than an array comprising rows and columns, for example, as latches or switches. The Examiner recites that FIG. 5A of Appellants is an example of a transistor addressed by rows and columns. Appellants note that while the transistor of FIG. 5A may be addressed by rows and columns, it is not necessarily so addressed, by may function, for example, outside of an array and/or not connected to rows and/or columns.

In rejecting claim 25, the Examiner said to see the rejection to claims 1-2. Claim 25 includes limitations similar to claim 1 and Appellants apply the same arguments as asserted for claim 1.

Conclusion

All of the pending claims following entry of the amendments, i.e., claims 1-31, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner or the Appeal Board has any further suggestions for expediting allowance of this application, the Examiner and the Appeal Board are invited to contact the undersigned at the telephone number indicated below.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

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Date: July 31, 2009

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APPENDIX

1. A method for programming a one time programmable memory, comprising the steps of:

obtaining an array of transistors; and

programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps.

2. The method of claim 1, wherein said programming step further comprises the step of applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

3. The method of claim 1, wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors.

4. The method of claim 3, wherein said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors.

5. The method of claim 3, further comprising the step of detecting said programmed at least one of said transistors by sensing said change in said threshold voltage of said at least one of said transistors.

6. The method of claim 5, wherein said detecting step further comprises the steps of raising a source terminal for each of said array of transistors to a positive potential; raising a gate terminal for all transistors along a selected row to a positive potential and detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential.

7. The method of claim 1, wherein said altered characteristic is a change in a saturation current of said at least one of said transistors.

8. The method of claim 7, wherein said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

9. The method of claim 7, further comprising the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors.

10. The method of claim 7, wherein said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive potential; raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay of at least one column in said array of transistors.

11. A one time programmable memory, comprising

an array of transistors, wherein at least one of said transistors is programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps; and

a circuit for sensing said altered characteristic of said at least one of said transistor.

12. The one time programmable memory of claim 11, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

13. The one time programmable memory of claim 11, wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors.

14. The one time programmable memory of claim 13, wherein said at least one of said transistors is programmed by applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors.

15. The one time programmable memory of claim 13, wherein said circuit senses said change in said threshold voltage of said at least one of said transistors.

16. The one time programmable memory of claim 15, wherein said circuit raises a source terminal for each of said array of transistors to a positive potential; raises a gate terminal for all transistors along a selected row to a positive potential and detects whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate potential.

17. The one time programmable memory of claim 11, wherein said altered characteristic is a change in a saturation current of said at least one of said transistors.

18. The one time programmable memory of claim 17, wherein said at least one of said transistors is programmed by applying a stressful voltage to a source and a gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

19. The one time programmable memory of claim 17, wherein said circuit senses said change in said saturation current of said at least one of said transistors.

20. The one time programmable memory of claim 17, wherein said circuit raises a voltage on at least one column in said array of transistors to a positive potential; raises a gate terminal of each transistor in a selected row to a positive potential and evaluates a rate of voltage decay of at least one column in said array of transistors.

21. A one time programmable memory element, comprising

at least one transistor that is programmed using hot carrier transistor aging to alter a transistor characteristic, wherein the hot carrier aging comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps; and

a circuit for sensing said altered characteristic of said transistor.

22. The one time programmable memory element of claim 21, wherein said altered characteristic is a change in a saturation current of said transistor.

23. The one time programmable memory element of claim 21, wherein said altered characteristic is a change in a threshold voltage of said transistor.

24. A memory cell, comprising only one transistor, wherein said transistor comprises:

a source region;

a drain region;

a channel region;

one silicon-dioxide gate insulator layer; and

one gate electrode layer.

25. The memory cell of claim 24, wherein the memory element is a one time programmable memory element programmed using a hot carrier transistor aging technique to alter a characteristic of said transistor, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps.

26. The memory cell of claim 24, further comprising a plurality of said memory cells arranged in an array of rows and columns.

27. An integrated circuit, comprising:

a one time programmable memory, comprising

an array of transistors, wherein at least one of said transistors is programmed using hot carrier transistor aging to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps; and

a circuit for sensing said altered characteristic of said at least one of said transistor.

28. The integrated circuit of claim 27, wherein said at least one of said transistors is programmed by applying a stressful voltage to said at least one of said transistors to cause said hot carrier transistor aging.

29. The integrated circuit of claim 27, wherein said altered characteristic is a change in a threshold voltage of said at least one of said transistors.

30. The integrated circuit of claim 27, wherein said circuit senses said change in said threshold voltage of said at least one of said transistors.

31. The integrated circuit of claim 27, wherein said altered characteristic is a change in a saturation current of said at least one of said transistors.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.